Digital Design Final Exam And Answers

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Digital Design Final Exam Study Guide Flashcards | Quizlet Start studying DIGITAL DESIGN FINAL EXAM REVIEW Learn vocabulary, terms, and more with flashcards, games, and other study tools Final Examination ENEL 353 Final Examination - Fall 2008 Page 5 of 12 (d) [6 marks] Re-design the circuit in Fig 2 using only 2-to-1 multiplexers

14:332:231 DIGITAL LOGIC DESIGN
DIGITAL LOGIC DESIGN Ivan Marsic, Rutgers University Electrical & Computer Engineering Fall 2013 2o 3f 0 Organizational Matters (1) – Final Exam 30 % – Random Quizzes 10 % 3 5o 3f 0 Source: Wikipedia 6o 3f 0 Source: Wikipedia 4 7o 3f 0 Clock Rate Grows Exponentially Year 1 10 100 1,000

Written exam with solutions IE1204-5 Digital Design Friday ...
Written exam with solutions IE1204-5 Digital Design Friday 15/1 2016 1400-1800 General Information Examiner: Ingo Sander Teacher: Kista, William Sandqvist tel 08-7904487 Teacher: Valhallavägen, Ahmed Hemani 08-790 4469 Exam text does not have to be returned when you hand in your writing Aids: No aids are allowed! The exam consists of three

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Sample Final Exam Solutions - uidaho.edu

Digital Logic Session 44; Page 1/5 Spring 2003 COE/EE 243 Sample Final Exam From Fall 98 Solutions Show your work Do NOT use a calculator! 1 (9 pts) Complete the following table of equivalent values Binary Octal Decimal Hexadecimal 10110011 1314 111875 B3 1110111111101 3577 2999 1DFD 11011010011 3323 27 19 64 1B4C 2 (12 pts

Midterm Exam - CAE Users

ECE 551 Digital System Design and Synthesis Midterm Exam Thursday, October 24, 2002 1:00--2:15PM (75 minutes) Instructions: 1 Open textbook examination, plus two 8 5x 11 note sheets allowed 2 Five points penalty if fail to enter name or ID number 3 No one shall leave room during last 5 minutes of the examination 4 Upon announcement of

Final Exams Review

ECE124 Digital Circuits and Systerns, Final Review, Spring Z0ll [Q1]Forthefollowing clocked sequential circuitwith one input (X)and one output (Z): 1 Drive a state table and draw a state diagram for the circuit 2 Redesign this circuit by replacing the Qr flip-flop (ie the D flip-flop holding Q1 state) with a JK flip- flop, and the Qz flip-flop with a T flip-flop

ECE380: Digital Logic Sample Exam 2 (KEY)

ECE380: Digital Logic Sample Exam 2 (KEY) The exam will be closed book and closed notes The following questions are representative of the type of questions that will be on the exam The exam will cover the lectures 12 and 14-26 from the class notes A sheet showing Boolean theorems will …

EXAM 1 SOLUTIONS - course.ece.cmu.edu

• This exam lasts 1 hour 50 minutes • If you make a mess, clearly indicate your final answer • For questions requiring brief answers, please provide brief answers Do not write an essay You can be penalized for verbosity • Please show your work when needed We …

Solutions

ICS 151 Digital Logic Design, Spring Quarter 2006, Final Page 8 Q2: FSM Design – Moore and Mealy Machines [30 points] We want to design a non-resetting sequence detector using a finite state machine with one input X and one output Y The FSM asserts its output Y when it recognizes the following input bit sequence: "1101"

Written exam with solutions for IE1204/5 Digital Design ...

Written exam with solutions for IE1204/5 Digital Design Monday 27/10 2014 900-1300 General Information Examiner: Ingo Sander Teacher: Elena Dubrova /William Sandqvist, tel 08-7904487 Exam text does not have to be returned when you hand in your writing Aids: No aids are allowed!

Decoders, Encoders, Multiplexers, Demultiplexers ...

EECC341 - Shaaban #6 Final Review Winter 2001 2-20-2002 Encoders • If the a decoder's output code has fewer bits than the input code, the device is usually called an encoder eg 2n-to-n, priority encoders • The simplest encoder is a 2n-to-n binary encoder, where it has only one of 2n inputs = 1 and the output is the n-bit binary number corresponding to the active input

Digital Signal Processing Midterm 2 Solutions

Digital Signal Processing Midterm 2 Solutions Instructions • Total time allowed for the exam is 80 minutes • Please write your name and SID on every page of the exam • Some useful formulas: – N point Discrete Fourier Transform (DFT) X[k] = NX−1 n=0 x[n]e−j2πkNn – Inverse Discrete

Fourier Transform (IDFT) x[n] = 1 N NX−1 k=0 X[k

Introduction to Digital Logic with Laboratory Exercises

then how digital logic functions are constructed using those gates The concept of memory is then introduced through the construction of an SR latch and then a D flip-flop A clock is created to be used in a basic state machine design that aims to combine logic circuits with memory Target audience

Endicott College 9/21/2020 Office of the Registrar Fall ...

Fall 2020 Final Exam Schedule - Undergraduate College Special Note: There are several exam periods in which students could be scheduled for two exams Faculty and students need to work together to solve the problem for individual students or groups

CSE 30321 – Computer Architecture I – Fall 2010 Final Exam ...

Final Exam December 13, 2010 Test Guidelines: 1 Place your name on EACH page of the test in the space provided 2 Answer every question in the space provided If separate sheets are needed, make sure to include your name and clearly identify the problem being solved 3 Read each question carefully Ask questions if anything needs to be

Understanding Logic Design - University of Iowa

Many problems of logic design can be specified using a truth table Give such a table, can you design the logic circuit? Design a logic circuit with three inputs A, B, C and one output F such that F=1 only when a majority of the inputs is equal to 1 A B C F Sum of product form 0 0 0 0 F = ABC + ABC + ABC + ABC

CSE 140L Final Exam - Computer Science

CSE 140L Final Exam Prof Tajana Simunic Rosing Winter 2009 Do not start the exam until you are told to Turn off any cell phones or pagers Write your name and PID at the top of every page Do not separate the pages This is a closed-book, closed-notes, no- calculator exam You many only refer to one